Lecture 9: AC-DC three-phase conversion

Saturday, 21 May 2022 1:07 PM

Three-phase rectifiers are commonly used in industry to produce a DC voltage and current for large loads.

We will look at uncontrolled and then controlled full-wave three-phase rectifiers.

Before that, a quick revision of three-phase systems [ElH08, Sec. 2.2] follows. The course [EEET 4057 Power System Fundamentals] has more details.

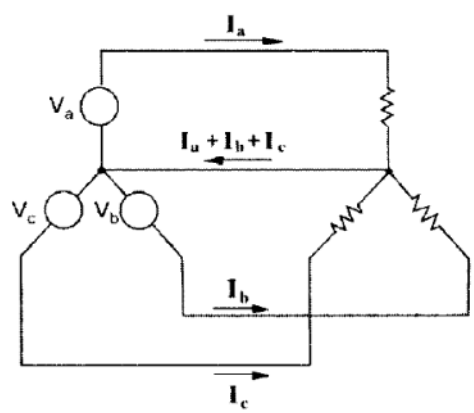
A *balanced* three-phase voltage system consists of three single-phase voltages with the same magnitude and frequency but time-displaced from one another by 120°.

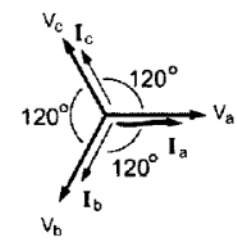
The adjacent configuration is a Y connection.

- The common terminal n is called the *neutral* or *star point*.

The three-phase voltage is said to have the *phase sequence abc*.

- This is important for applications such as three-phase induction motors, where the phase sequence determines whether the motor turns clockwise or counterclockwise.





$\vec{V}_{ab}$, $\vec{V}_{bc}$, and $\vec{V}_{ca}$ are the *line voltages*, while $\vec{V}_a$, $\vec{V}_b$, and $\vec{V}_c$, are the *phase voltages*.

If the phase voltages have magnitude V_{ph}, and the line voltages have magnitude V_L, then

$$\vec{V}_{ab} = \vec{V}_a - \vec{V}_b = V_{ph}(1 - \angle -120°) = \sqrt{3}V_{ph}\angle 30°$$
$$\Rightarrow V_L = \sqrt{3}V_{ph}.$$

Equivalently, $V_{ph} = V_L/\sqrt{3}$.

The line current (magnitude I_L) equals the phase current (magnitude I_{ph}).

Suppose $\vec{I}_a$ lags $\vec{V}_a$ by ϕ radians, then the *apparent power* is defined as

$$S \triangleq 3V_{a,rms}I^*_{a,rms} = 3V_{ph,rms}I_{ph,rms}\angle\phi$$
$$= \sqrt{3}V_{L,rms}I_{L,rms}\angle\phi$$
$$= \sqrt{3}V_{L,rms}I_{L,rms}\cos\phi + j\sqrt{3}V_{L,rms}I_{L,rms}\sin\phi\,.$$

real power

S is a complex number with a magnitude of

$$|S| = \sqrt{3}V_{L,rms}I_{L,rms}.$$

The *real power* is thus

$$P = \sqrt{3}V_{L,rms}I_{L,rms}\cos\phi\,.$$

1. Uncontrolled full-wave three-phase rectifiers

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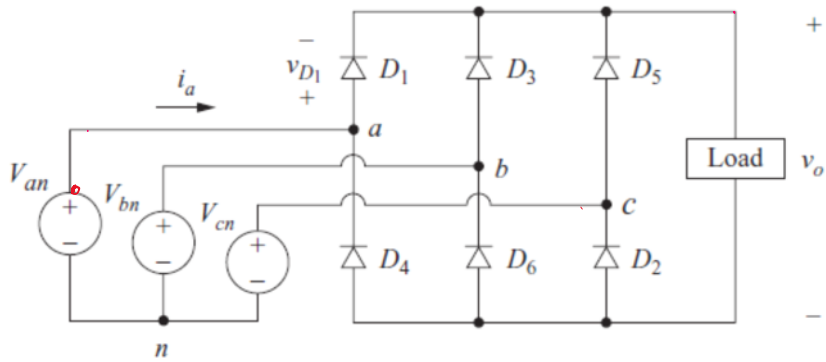
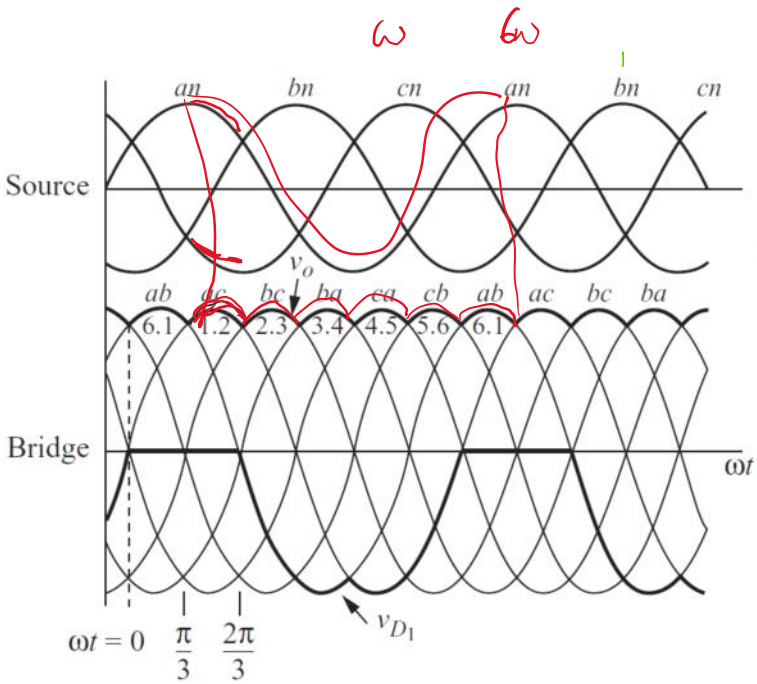
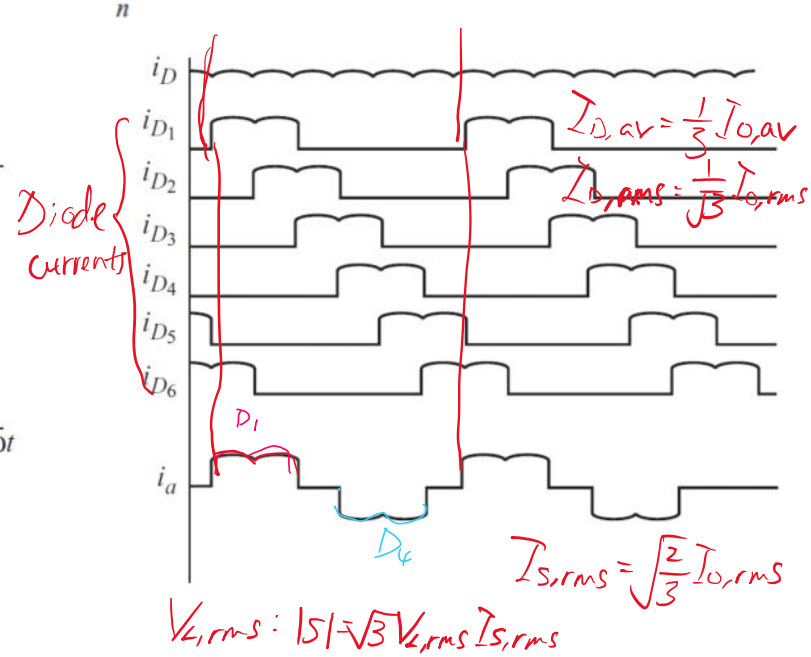
(6,1), (1,2), (2,3) . . . . .

Most basic circuit is the ***three-phase full-bridge rectifier*** ☞

Assume balanced three-phase voltage source with phase sequence a-b-c.







KVL around any loop tells us only one diode in the top half of the bridge *may* conduct at one time (D_1, D_3 or D_5, because when one is forward biased the other is reverse biased). The diode that is conducting will have its anode connected to the phase voltage that is highest at that instant.

KVL also tells us only one diode in the bottom half of the bridge *may* conduct at one time (D_2, D_4 or D_6). The diode that is conducting will have its cathode connected to the phase voltage that is lowest at that instant.

The observations above imply each of these pairs cannot conduct at the same time: (D_1 and D_4), (D_3 and D_6), (D_5 and D_2).

Choosing two out of three alphabets (abc), v_o is one of $\binom{3}{2} = 3$ line-to-line voltages of the source, e.g., when

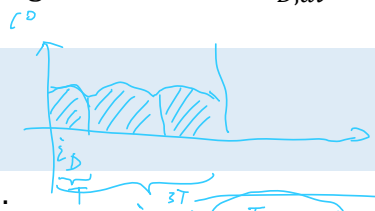
D_1 and D_2 are on, the output voltage is v_{ac}.

A transition of the highest line-to-line voltage takes place every $\pi/3$ rad.

- The fundamental frequency of the output voltage is 6ω, where ω is the frequency of the three-phase source.
- Six transitions per period of the source voltage gives the circuit the name ***six-pulse rectifier***.

The diodes conduct in pairs (6,1), (1,2), (2,3), (3,4), (4,5), (5,6), (6,1), ... Diodes turn on in the sequence 1, 2, 3, 4, 5, 6, 1, ... Since each diode conducts one-third of the time, the average diode current $I_{D,av}$, the rms diode current $I_{D,rms}$ and the rms source current $I_{S,rms}$ can be found as

(1.1)
$$I_{D,av} = \frac{1}{3} I_{o,av}, \qquad I_{D,rms} = \frac{1}{\sqrt{3}} I_{o,rms}, \qquad I_{S,rms} = \sqrt{\frac{2}{3}} I_{o,rms}.$$



The third equality can be derived by observing the waveforms of i_o and i_a.

$i_D = \sqrt{\frac{1}{3T}\int_0^T i^2 dt} = i_o$

$i_o = \sqrt{\frac{1}{T} \cdot \int_0^T i^2 dt}$

$i_D = \sqrt{\frac{T}{3}}\, i_o$

Apparent power if rms line voltage is $V_{L,rms}$:

(1.2) $$|S| = \sqrt{3} V_{L,rms} I_{S,rms}.$$

Note the phase voltage is $V_{ph} = \frac{V_L}{\sqrt{3}}$.

The output voltage can be represented using a Fourier series:

(1.3)
$$v_o(t) = \frac{3V_L}{\pi} - \sum_{n=6,12,\ldots}^{\infty} V_n \cos(n\omega t),$$

DC term

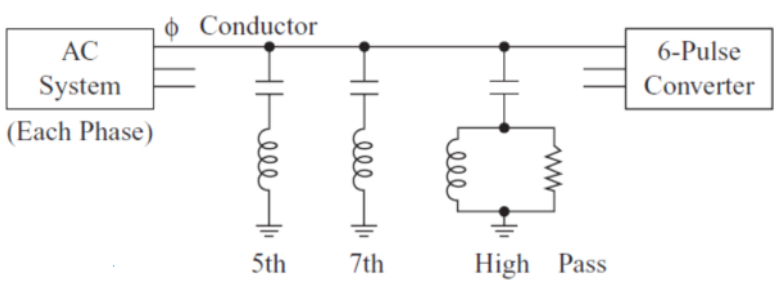
where

$$V_L = \sqrt{2} V_{L,rms}, \qquad V_n = \frac{6V_L}{\pi(n^2-1)}.$$

In many applications, a load with series inductance results in a load current that is essentially flat [Har11, pp. 146-147].

The Fourier series of the currents in phase a of the AC line consists of terms at the fundamental frequency of the AC system and harmonics of order $6k \pm 1$, $k = 1,2,3, \ldots$

- The fifth and seventh harmonics are the two lowest and are the strongest in amplitude.
- Hence, filters such as this are frequently necessary to prevent these harmonics from entering the AC system:



- Higher-order harmonics are attenuated (not eliminated) with the high-pass filter.
- Filter components are chosen such that the impedance to the power system frequency is large.

For an example on how to analyze the six-pulse rectifier, refer to Tutorial 9.

2. Controlled full-wave three-phase rectifiers

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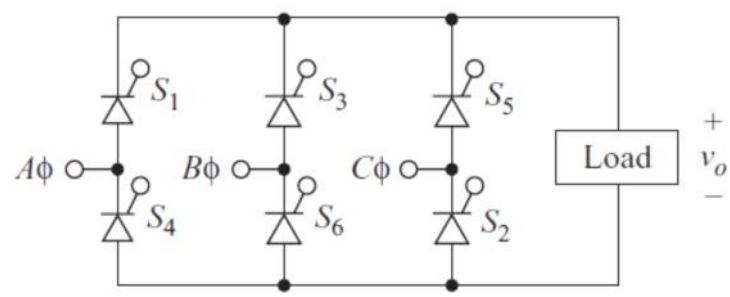
Replacing the diodes with SCRs in the full-bridge rectifier, we get the phase-controlled full-bridge rectifier ☞

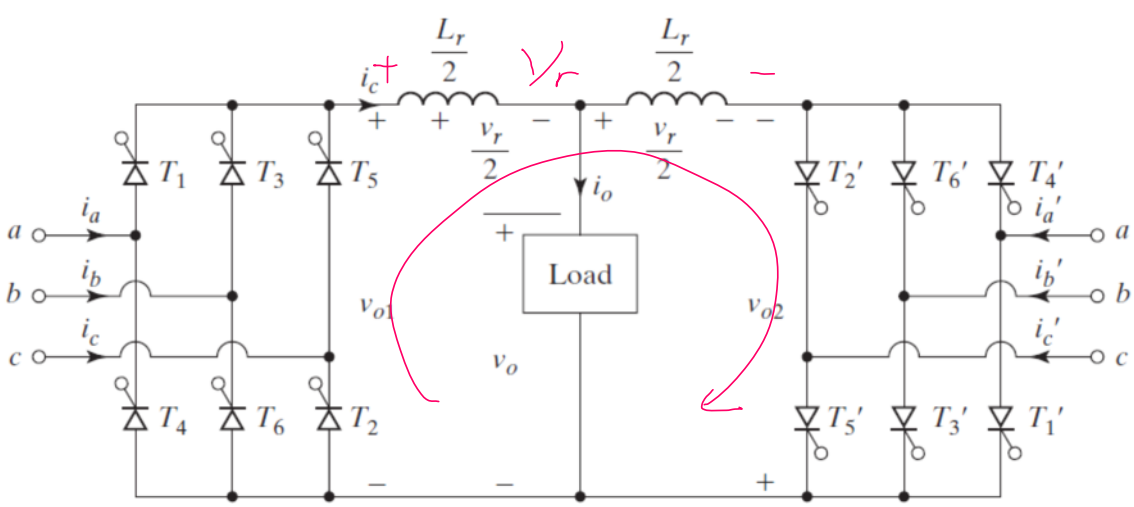


DC output voltage now becomes

(2.1) $$V_o = \frac{3V_L}{\pi}\cos\alpha\,.$$

As we have seen before in the previous lecture, power factor is a common issue among phase-controlled rectifiers.

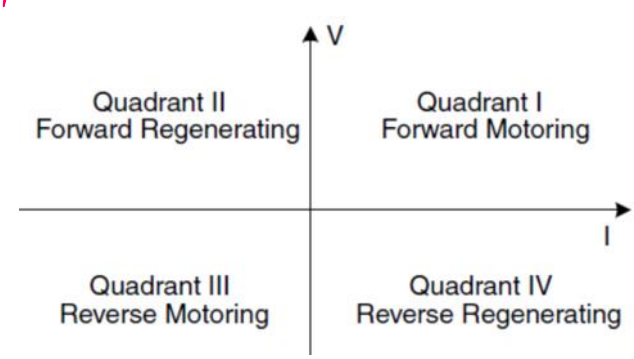
So far we have only discussed *full converters*. The following is an example of a three-phase *dual converter* [Ras14, Sec. 10.5]:



$-V_{o1} + V_r - V_{o2} = 0 \Rightarrow V_r = V_{o1} + V_{o2}$

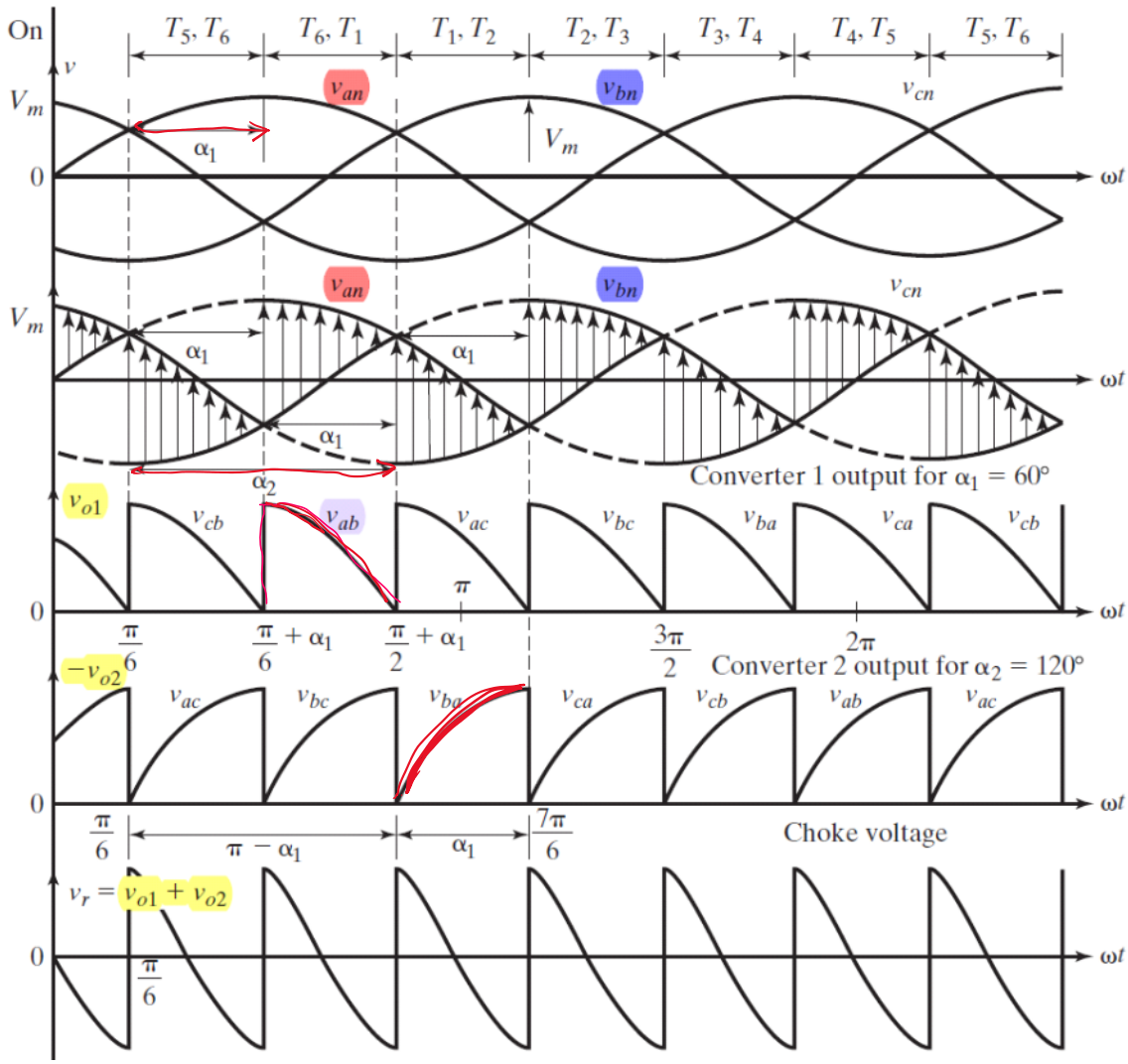
Converters like the above are used to enable the four-quadrant operation of variable-speed drives, and are extensively used in applications up to the 2 MW level.

- Four-quadrant ⇒ power can be fed to and extracted from the load ⇒ can realize acceleration, deceleration and regeneration



The back-to-back connected converters are controlled in this manner: if the delay angle of converter 1 is α_1, the delay

angle of converter 2 is $\alpha_2 = \pi - \alpha_1$; see below 👇



The output voltage differences between the converters cause a circulating current to flow between them, and is limited by the *circulating reactor* L_r [Ras14, Sec. 10.5].

The inductor facilitates smooth reversal of load current during the changeover from one quadrant operation to another.

- This provides fast dynamic responses, especially for electrical motor drives.

3. Modern rectifiers

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This section involves both single-phase and three-phase power.

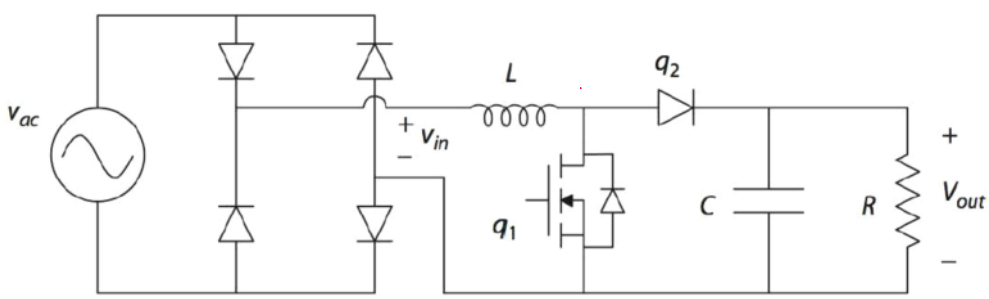
The linkage between line frequency and phase-controlled rectifiers leads to relatively large filters and tends to make low power levels inconvenient [Kre15, Sec. 4.5].

Another challenge lies in the linkage between output control and power factor: in a phase-controlled rectifier, the power factor is proportional to $\cos\alpha$ and degrades as decreased output is desired.

The alternative to ***line-commutated rectification*** (what we have discussed so far) is ***active rectification***, which uses an *uncontrolled diode bridge* (usually filtered with a capacitor) followed by a DC-DC converter.

In effect, the wide voltage variation out of the uncontrolled bridge is treated as a slowly varying DC source and then processed through a much faster DC-DC converter that varies its duty cycle/ratio to correct the result — this hints at the importance of *control*.

The basic active rectifier has this topology called the ***boost active rectifier*** [Kre15, FIGURE 4.47]:



The bridge rectifier provides a source that varies from 0 to V_m, where V_m is the magnitude of V_{ac}.

Reason for connecting the bridge rectifier to a boost converter instead of a buck converter:

- If the bridge rectifier is connected to a *buck* converter, there will be times when the input is too low.

- If the bridge rectifier is connected to a *boost* converter, the output is always higher than the input, so a boost converter can provide the desired result if its output is set to at least V_m (i.e., highest value of the input voltage). From Lecture 5 (see knowledge base entry), the duty cycle can be calculated as
$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{|V_m \sin(\omega t)|}{V_m} = 1 - |\sin(\omega t)|.$$
Note $|V_m \sin(\omega t)|$ is the output of the bridge rectifier. D must be calculated in real time by a controller.

  Since DC-DC converters operate at 20 kHz or higher, the 50× 2 Hz or 60× 2 Hz variation of the bridge output appears as a low-frequency disturbance to the controller.

The PWM method associated with the boost converter has two major advantages 👍:

Main disadvantage 👎:

The PWM method associated with the boost converter has two major advantages 👍:

1. The output voltage can be chosen not just to match V_m but instead to match the highest expected voltage. The converter then supports extreme input ranges, such as the 100 V to 265 V rms values supported by many present small power supplies.

2. The basic circuit scales down well, even if it may enter DCM. Converters operating at just a few watts can be supported with far smaller circuits and less storage than with classical rectifiers.

The PWM controller is expected to implement ***power factor correction*** (PFC) to achieve a high power factor.

Objectives of PFC [LY18, Sec. 4.1; EKN09, Sec. 3.1; KS83; ONS14]:

1. Reducing the phase difference between the line voltage and current; see figure 👉

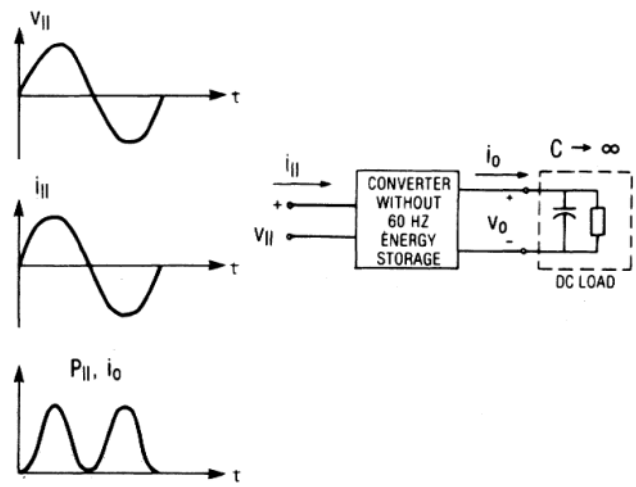
2. Shaping the line current to a sinusoidal waveform, i.e., to achieve low *total harmonic distortion* (THD, introduced in Tutorial 1) of the current.

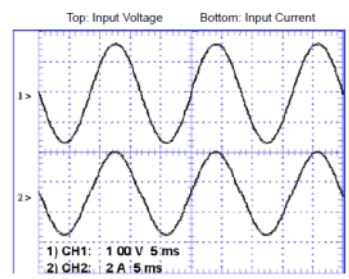
   In fact, the international standards IEEE 519-2014, IEC 61000-3-2 and EN61000-3-2 have restrictions on current harmonics in modern rectifiers.

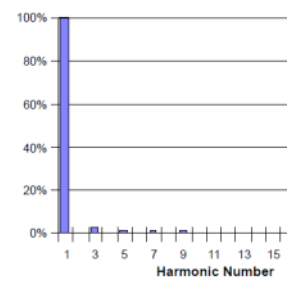
Main disadvantage 👎:

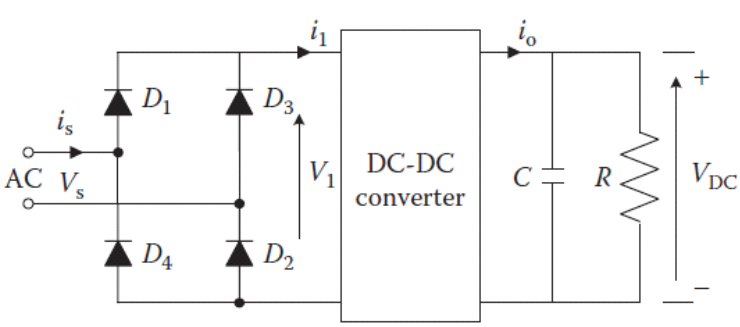
1. Output voltage must be relatively high. A 265 V rms input has a peak value of 375 V, and boost active rectifiers often operate at a nominal 400 V output.

   For a low-voltage output, an additional step-down converter is necessary, at the expense of cost and efficiency loss.









In general, a rectifier with the adjacent topology is known as a ***PFC rectifier***.

PFC works by modulating the DC current on the bridge output so as to retrieve a practically sinusoidal current (i.e., with low THD) from the AC source [AMA14, Sec. 16.1].

For supplementary information, Texas Instruments has some PFC-related training videos, including:

1. Power factor correction (PFC) circuit basics: introduction and why PFC matters
2. Power factor correction (PFC) basics and design considerations

Secs. 3.1-3.2 discuss single-phase PFC and three-phase PFC respectively.

$u=1$ $V_o = V_s = L\frac{di_{in}}{dt}$

$u=0$ $V_{in} - V_o = V_L$.

Secs. 3.1-3.2 discuss single-phase PFC and three-phase PFC respectively.

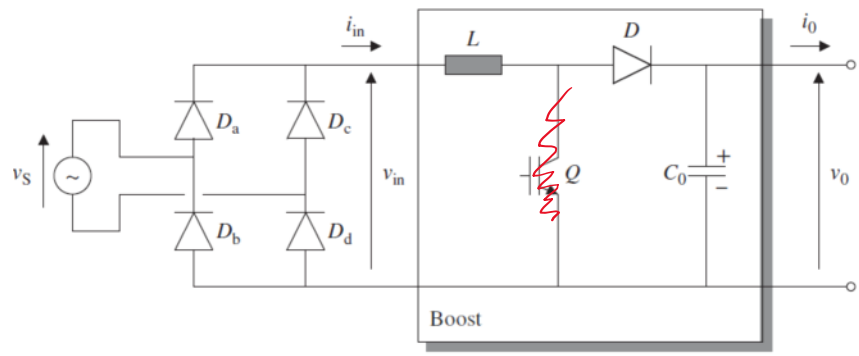
$u=1$: $V_{in} = V_L = L\frac{di_{in}}{dt}$

$u=0$: $V_{in} - V_o = V_L = L\frac{di_{in}}{dt}$

$V_{in} - (1-u)V_o = L\frac{di_{in}}{dt}$

3.1 Single-phase PFC

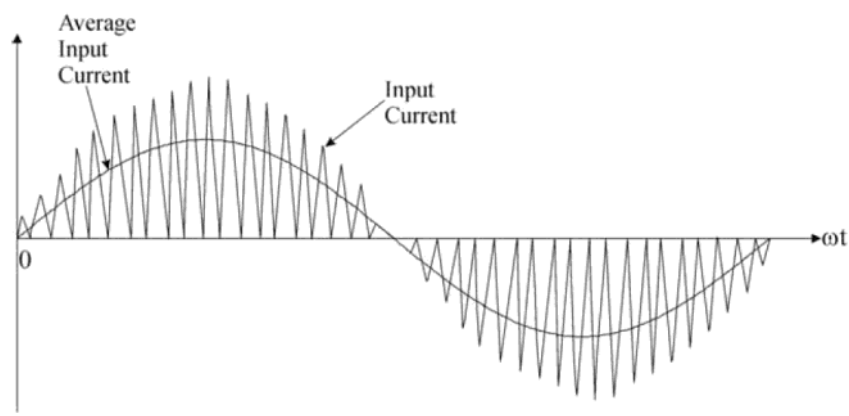
Examples of single-phase PFC include boost, bridgeless and totem-pole [Bla18, Sec. 13.3.3], with boost being the most basic and potentially most prevalent; see figure ☞



Three operation modes [DDS15; Ras18, pp. 219-222]:

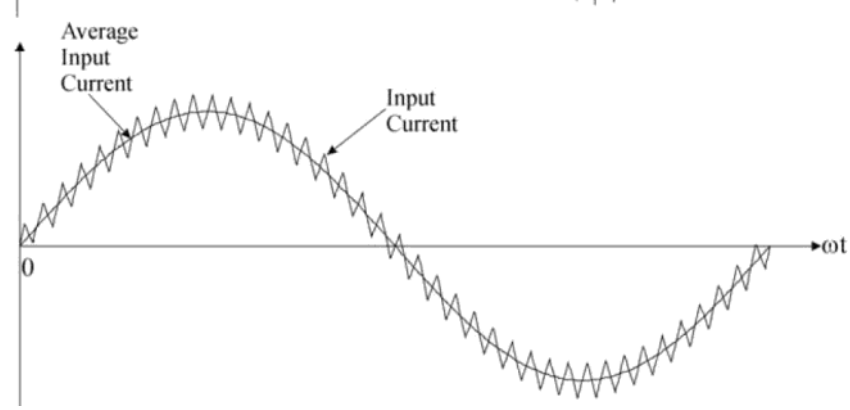
Critical Conduction Mode (CrCM):

- Also called *boundary conduction mode*.
- Inductor current is always zero before the switch is turned on, minimizing turn-on losses.
- Reverse recovery performance of boost diode not crucial.
- Watch TI's [“PFC Circuit Basics: The CrCM Boost Converter”](#).



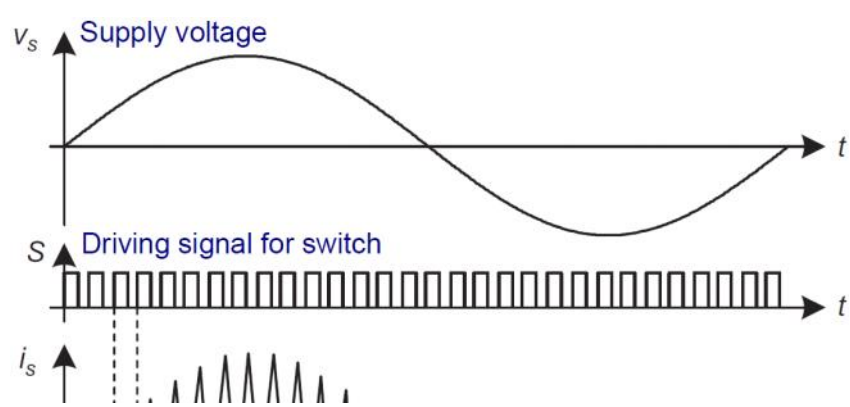
Continuous Conduction Mode (CCM):

- Low voltage swing results in low conduction losses.
- Low ripple current results in low inductor-core losses.
- Overall, higher PF and lower THD than CrCM.
- But since i_L does not fall to zero, a fast-recovery diode is needed for quick turning off; see waveform.
- Watch TI's [“PFC Circuit Basics: The CCM Boost Converter”](#).



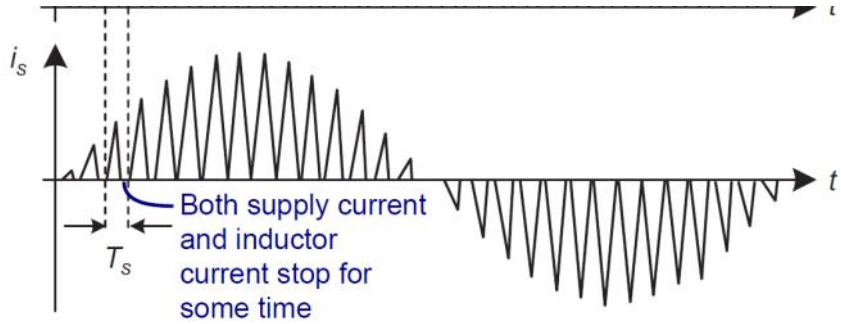
Discontinuous Conduction Mode (DCM):

- Switch is turned on when the inductor current reaches zero and turned off when the inductor current meets the desired reference input.
- The reason for using different modes comes down to a tradeoff between cost and efficiency.
- Although filter inductor can be smaller in DCM, the conversion ratio is dependent on

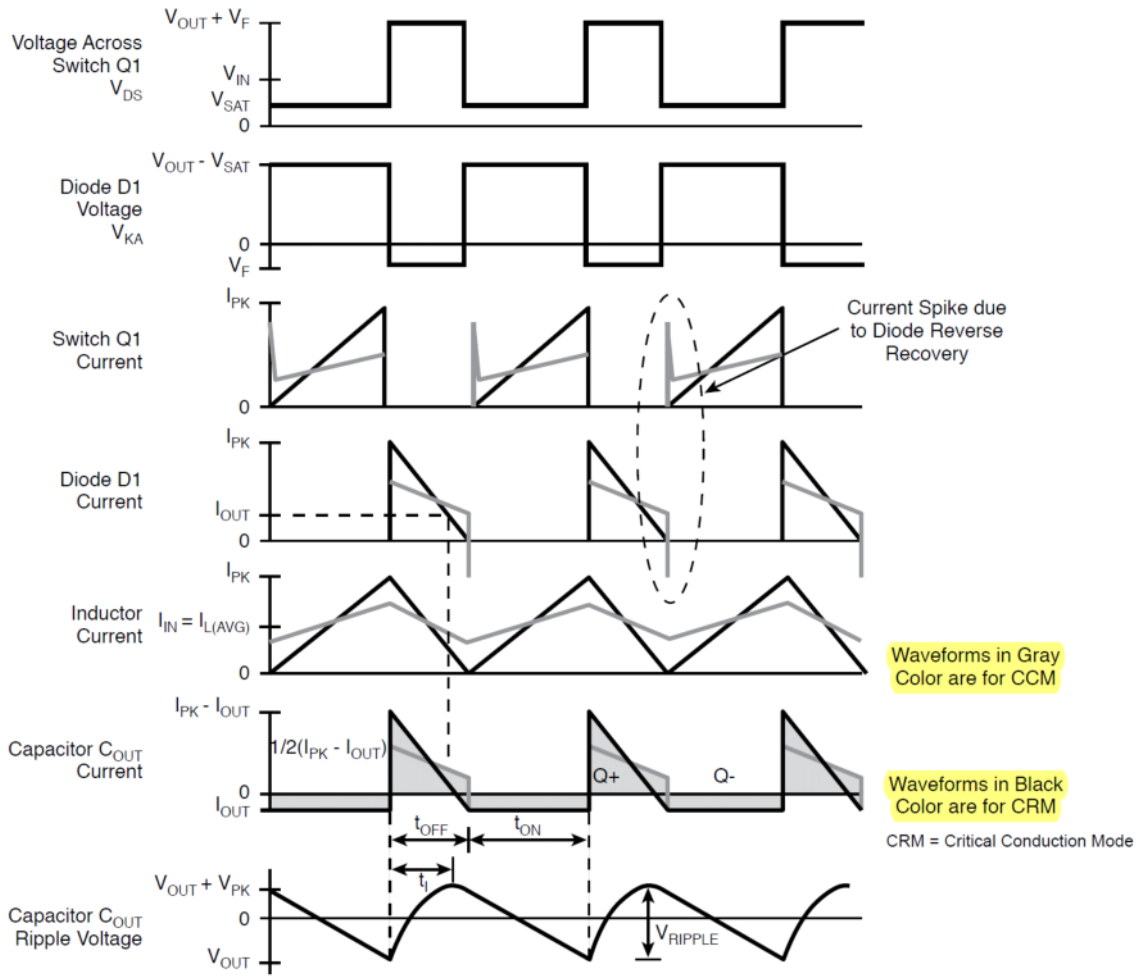


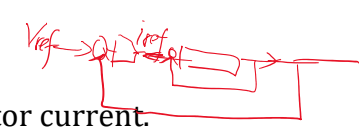
and efficiency.

- Although filter inductor can be smaller in DCM, the conversion ratio is dependent on the load condition and high EMI levels may result.
- More suitable for low-power applications.



Waveform sketches supplementing discussion of operation modes [Pow17, Figure 22]:

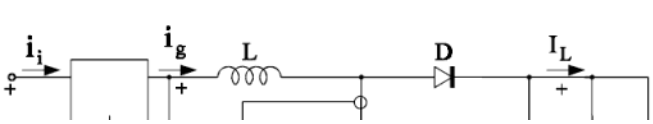




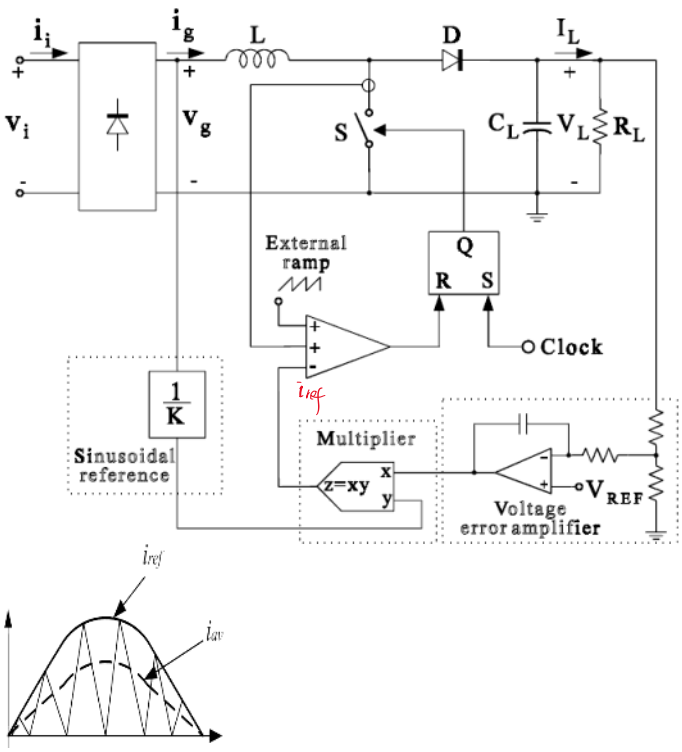
Relevant control laws are called *current-mode control* [She07].

- An ideal current-mode converter is only dependent on the DC or average inductor current.
- Cascade control is typical: it contains an inner current control loop and an outer voltage control loop.
- The higher-bandwidth inner current loop turns the inductor into a voltage-controlled current source, effectively removing the inductor from the outer voltage control loop at DC and low frequencies.
- Watch TI's [“Power factor correction (PFC) classification and control laws”](#).

Current-mode control methods for modulating the inductor current include [She07; ONS14; RST94; DDS15; DB15, Sec. 7.9.1]:



Peak current-mode control or **peak current control**: Compares inductor current to a reference signal obtained from an input voltage sample, and turns off the



Peak current-mode control or **peak current control**: Compares inductor current to a reference signal obtained from an input voltage sample, and turns off the switch when the current sample equals the reference.

Advantages 👍:

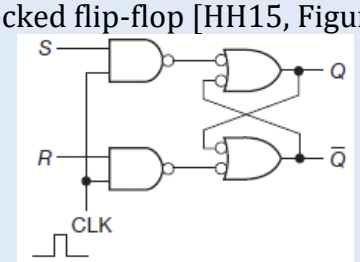
- Only switch current needs to be sensed (see adjacent figure), for which a current transformer can be used, avoiding the losses associated with a sensing resistor.
- Fast closed-loop transient response.
- Natural cycle-by-cycle current limit.
- Fixed switching frequency.

Disadvantages 👎:

- Control is sensitive to commutation noise (a spike for every turning on); spurious voltage fluctuations in the control circuit can turn off the switch inadvertently.
- Instability associated with presence of subharmonic oscillations at duty cycles greater than 50% (what happens when duty cycle → 1 for a boost converter?).

Details: SR latch

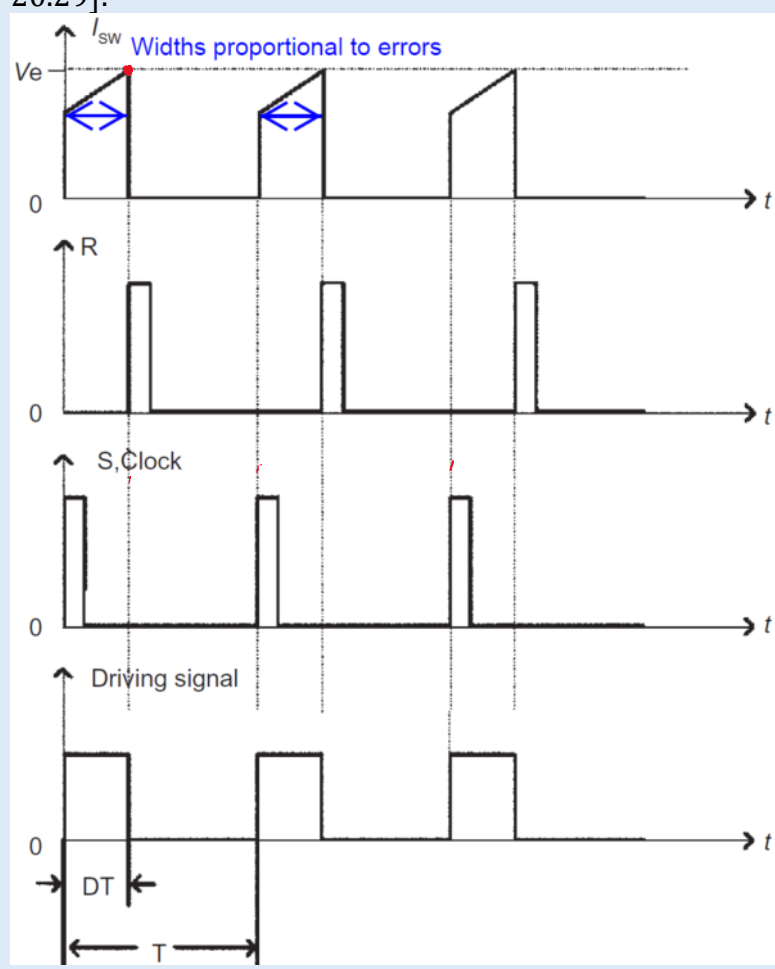
The operation of the SR latch (S=Set, R=Reset) would have been covered in an early undergraduate course. An approximation of the SR latch is the following clocked flip-flop [HH15, Figure 10.54]:

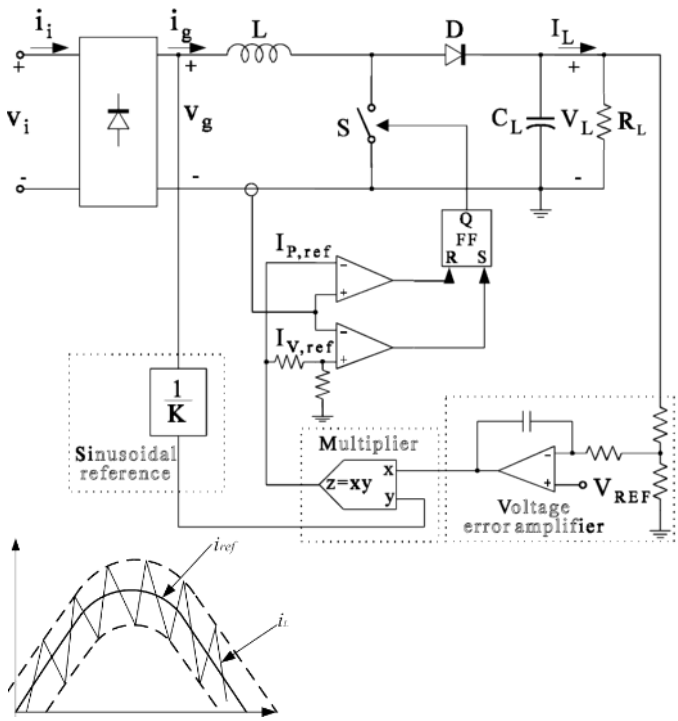


If Q_n designates the current output state, and Q_{n+1} the next, then the following truth table applies:

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	indeterminate

An example of a driving signal sequence [Ras18, FIG. 20.29]:





Hysteresis current-mode control or **hysteresis current control**:
Two sinusoidal current references: one upper/peak, one lower/valley (see $I_{p,ref}$ and $I_{v,ref}$ in adjacent figure).

- $I_{p,ref}$ and $I_{v,ref}$ form a *hysteresis band*.
- Switch is turned on when inductor current goes below the hysteresis band, and turned off when inductor current goes above the hysteresis band.
- Works in CCM, so the same considerations for peak current control apply.

Advantages:

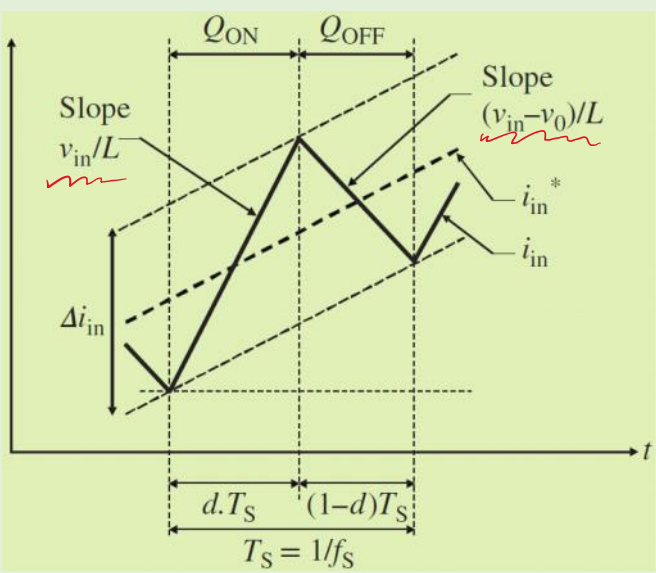
- Good transient response.

Disadvantages:

- Inductor current must be sensed.
- Control is sensitive to commutation noise.
- Variable switching frequency. To avoid excessively high switching frequency, the switch can be kept open near the zero crossing of the line voltage, but this introduces dead times in the line current.

Example 3.1

Consider hysteresis current trajectory below [AMA14, Sec. 16.2.1]:



Based on the symbols in the circuit diagram, derive a large-signal averaged model of the boost converter circuit, and thereby show that upward slope and download slope can indeed be expressed as shown above.

For simplicity of modeling,

Solution: Applying KVL to the inductor current,

$$v_{in} - (1-u)v_o = L\frac{di_{in}}{dt}$$

$$\Rightarrow i'_{in} = -\frac{1}{L}(1-u)v_o + \frac{1}{L}v_{in}$$

$$\Rightarrow \langle i'_{in}\rangle = -\frac{1}{L}(1-d)\langle v_o\rangle + \frac{1}{L}v_{in}.$$

$\frac{di_{in}}{dt} = \frac{V_{in}}{L}$ $u=1$

$\frac{di_{in}}{dt} = \frac{V_{in}-V_o}{L}$ $u=0$

The slopes of i_{in} when Q is ON and when Q is OFF are indeed v_{in}/L and $(v_{in} - v_o)/L$ respectively, as shown in the adjacent plot.

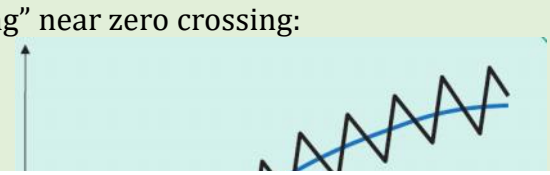
Applying KCL to the capacitor voltage,

$$C_o\frac{dv_o}{dt} = -i_o + (1-u)i_{in}$$

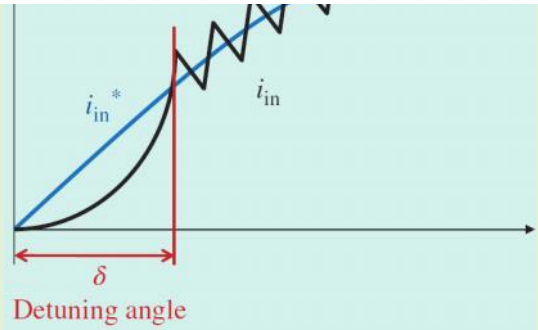
$$\Rightarrow v'_o = \frac{(1-u)}{C_o}i_{in} - \frac{1}{RC_o}v_o$$

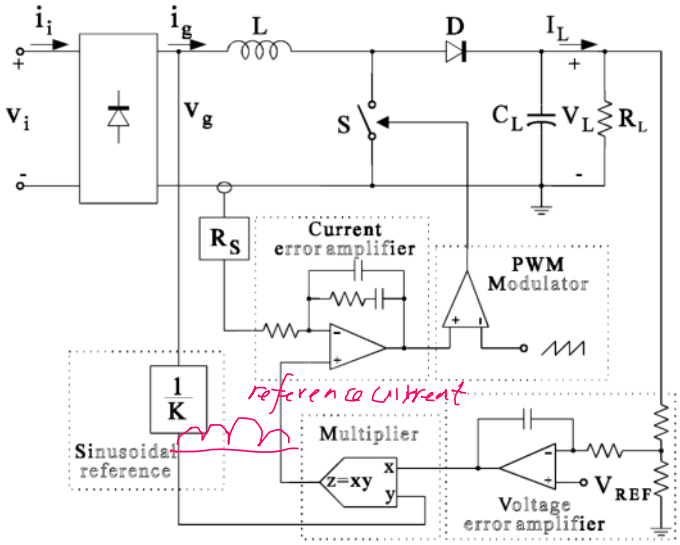
$$\Rightarrow \langle v'_o\rangle = \frac{(1-d)}{C_o}\langle i_{in}\rangle - \frac{1}{RC_o}\langle v_o\rangle.$$

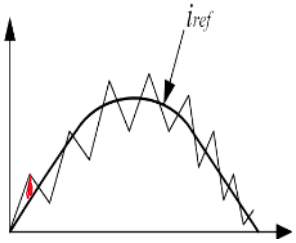
At this point, our model is complete. Additional info: i_{in} changes faster than i_{in}^* except during "control detuning" near zero crossing:



- Assume CCM.
- Let u be the switching function (1 when Q is ON, 0 when Q is OFF).
- Let d be the duty ratio.







Average current-mode control or **average current control**:
Inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator.

- Reference current generation same as peak current control (see adjacent figure).
- The inner current loop attempts to minimize the error between the average input current and its reference.
- Works in CCM, so the same considerations for peak current control apply.

Advantages:

- Current tracking can be achieved with high accuracy.
- Better input current waveforms than for the peak current control, since the duty cycle is close to one near zero crossings of the line voltage.
- Low sensitivity to commutation noises — one can even say excellent noise immunity — due to current filtering.
- Fixed switching frequency.

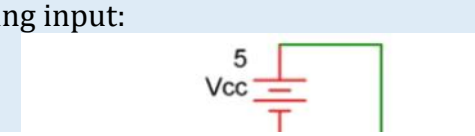
Disadvantages:

- Inductor current must be sensed.
- Complex control. Note "PWM Modulator" in average current control as opposed to "SR latch" in peak current control.

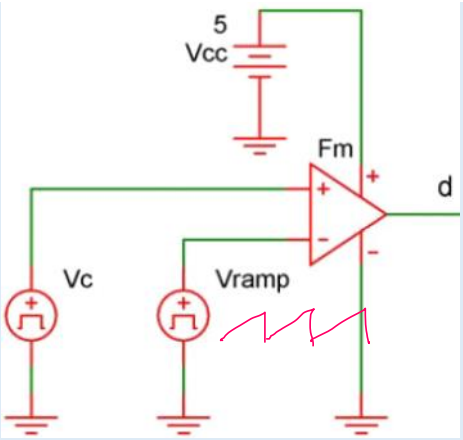
The pros (despite cons) popularize this control method.

Details: PWM

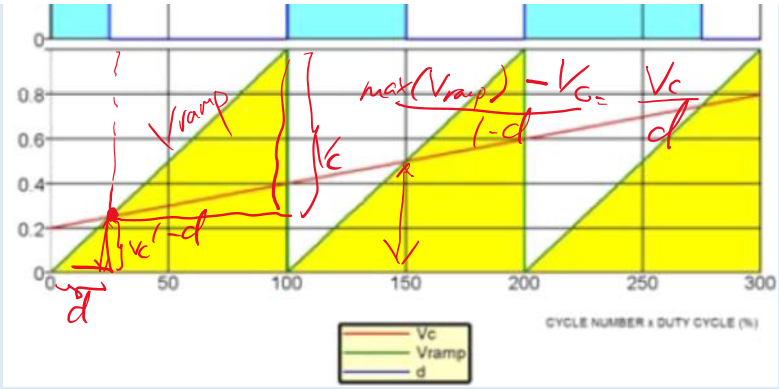
As part of PWM, a comparator is typically used to modulate the duty ratio [She07]. For fixed-frequency switching, a sawtooth voltage ramp (V_{ramp}) is applied to the inverting input, whereas a control/error signal (V_c) is applied to the non-inverting input:



Resultant waveforms (duty ratio d):



When $V_c > V_{ramp}$, the comparator outputs V_{cc}, turning *on* the associated switch; otherwise, the comparator outputs 0 V.



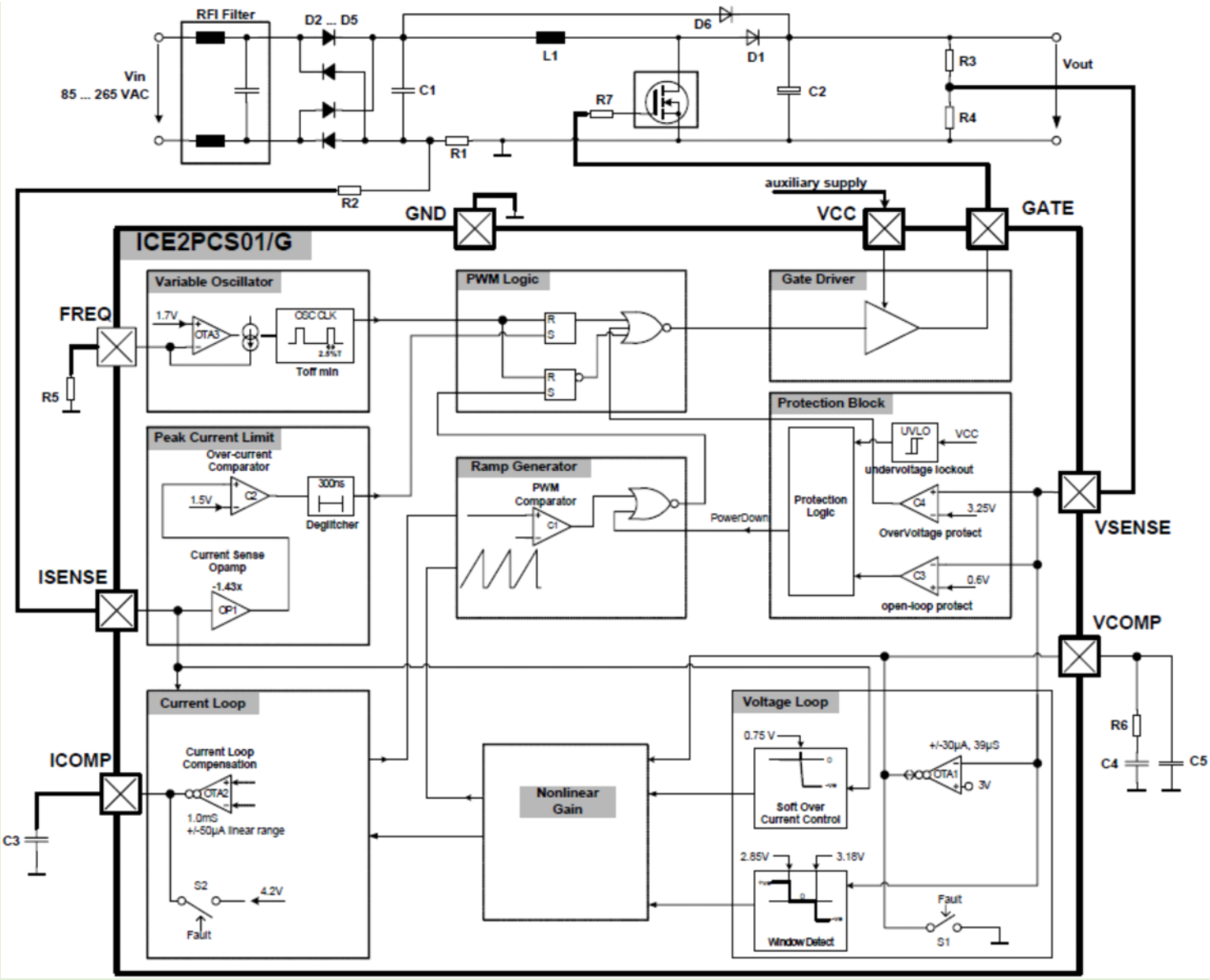
$$\frac{\max(V_{ramp}) - V_c}{1-d} = \frac{V_c}{d} \Rightarrow d = \frac{V_c}{\max(V_{ramp})}.$$

constant

Thus, by controlling V_c the desired duty ratio can be achieved.

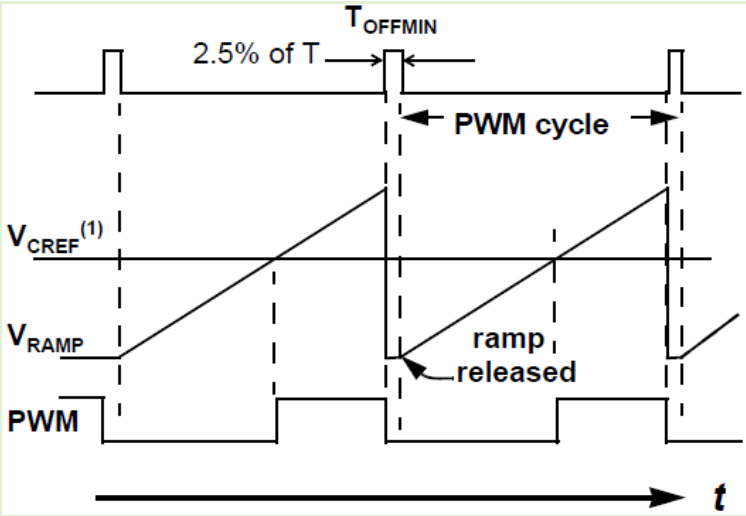
Example 3.2

An example of a commercial PFC controller is the Infineon Technologies ICE2PCS01 average current controller. Visible in the block diagram for the 8-pin controller IC below is a voltage loop in cascade with a current loop:



The current loop is of interest here:

- Inductor current is sensed by reading at pin ISENSE the voltage across R1.
- Compensation of the current loop happens at pin ICOMP (details omitted).
- PWM is performed by intersecting a ramp ☞ signal in the Ramp Generator block with the averaged inductor current at pin ICOMP.
- PWM cycle starts with gate turn-off for duration T_{OFFMIN}, before ramping commences.
- Once the ramp surpasses the average waveform, the comparator C1 turns *on* the driver stage through the PWM Logic block.
- Note in this case $1 - d \propto$ the voltage at pin ICOMP representing the average current.



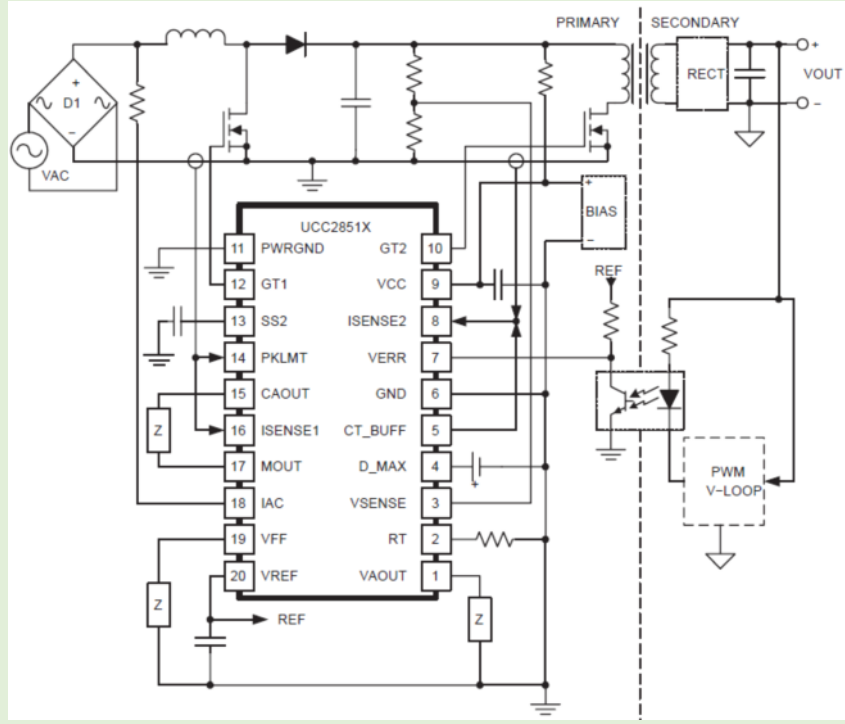
Example 3.3

Another example of a commercial PFC controller is the [Texas Instruments UCC28510 series](#) of combination PFC/PWM controllers for supporting IEC1000-3-2 harmonic reduction requirements for offline power systems.

The core of the PFC section is in a three-input *multiplier* that generates the reference signal for the line current.

The multiplier is highly linearized and capable of producing a low-distortion reference for the line current.

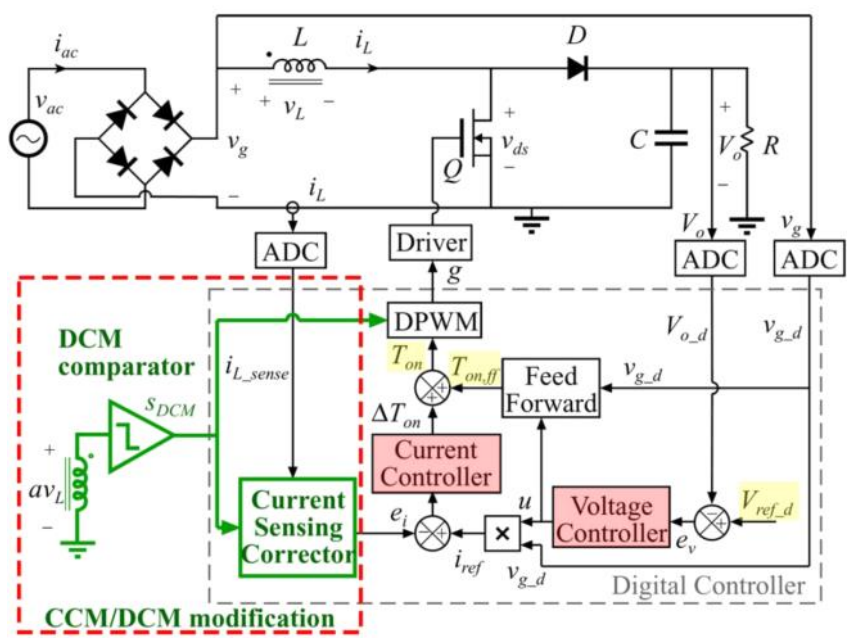
A low-offset, high-bandwidth *current error amplifier* ensures the inductor current (sensed through a resistor in the return path) follows the multiplier output command signal.



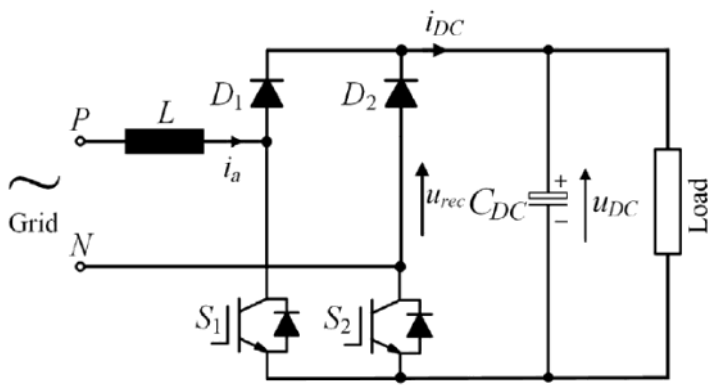
There are more sophisticated current-mode control schemes than the three main ones above.

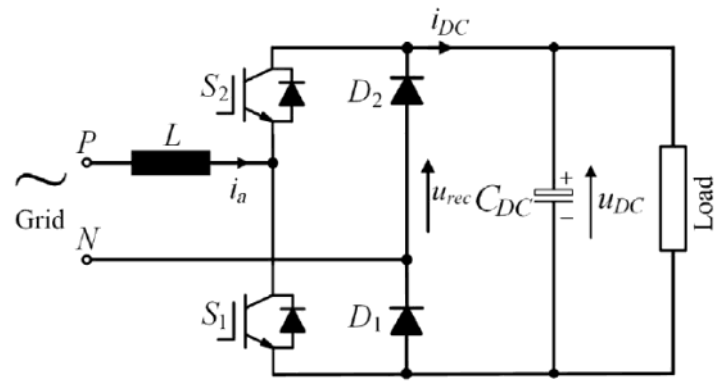
For example, Chen and Maksimović's predictive current control [CM10] is aimed at improving efficiency and reducing harmonic distortion in both CCM and DCM.

- Control architecture retains cascade control loop with inner current control and outer voltage control loops.
- Feedforward term $T_{on,ff}$ improves transient response, but depends on whether the circuit is in CCM or DCM.
- Control variable is the transistor on-time, T_{on}.



Besides the boost topology, there are many other kinds of PFC topologies, including:





Bridgeless PFC, also called dual-boost PFC [Bla18, Sec. 13.3.3]:

- Inductor relocated from output to input.
- Two diodes of the bridge rectifier are replaced with active power switches.
- Line current flows through only two semiconductors.
- Conduction loss is thus lower than the boost PFC.
- However, susceptible to common-mode noise (see knowledge base entry).
- More details in TI's training video on "PFC Circuit Basics: Bridgeless PFC".

Totem-pole PFC:

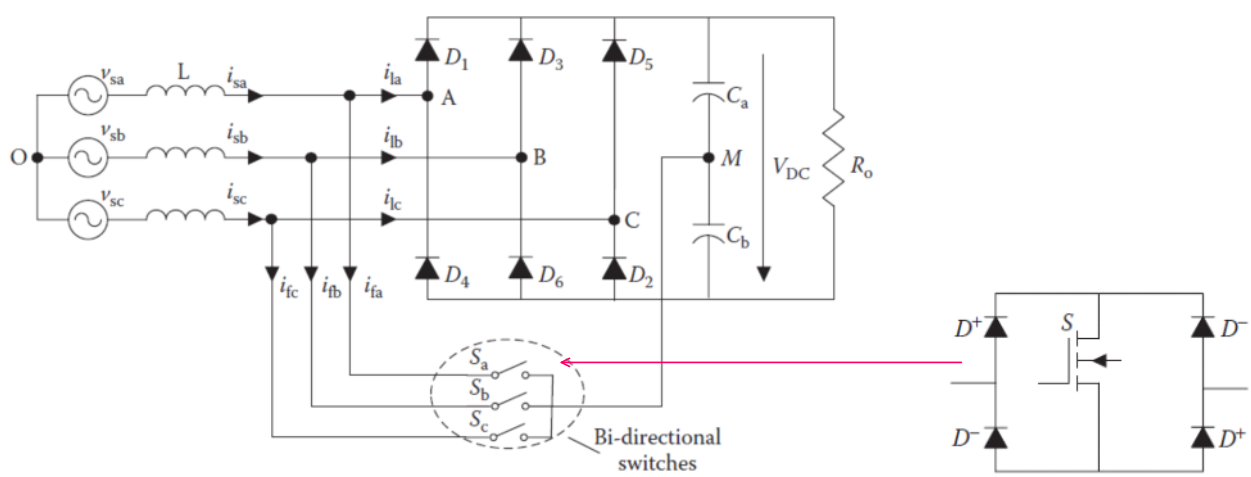
- Same number of components as bridgeless PFC.
- Switches arranged to enable bidirectional flow (i.e., bidirectional i_{DC}).
- Wide-bandgap material usually used for the diodes for energy efficiency.
- Also susceptible to common-mode noise like bridgeless PFC.

Boost PFC and totem-pole PFC are analyzed in the tutorial.

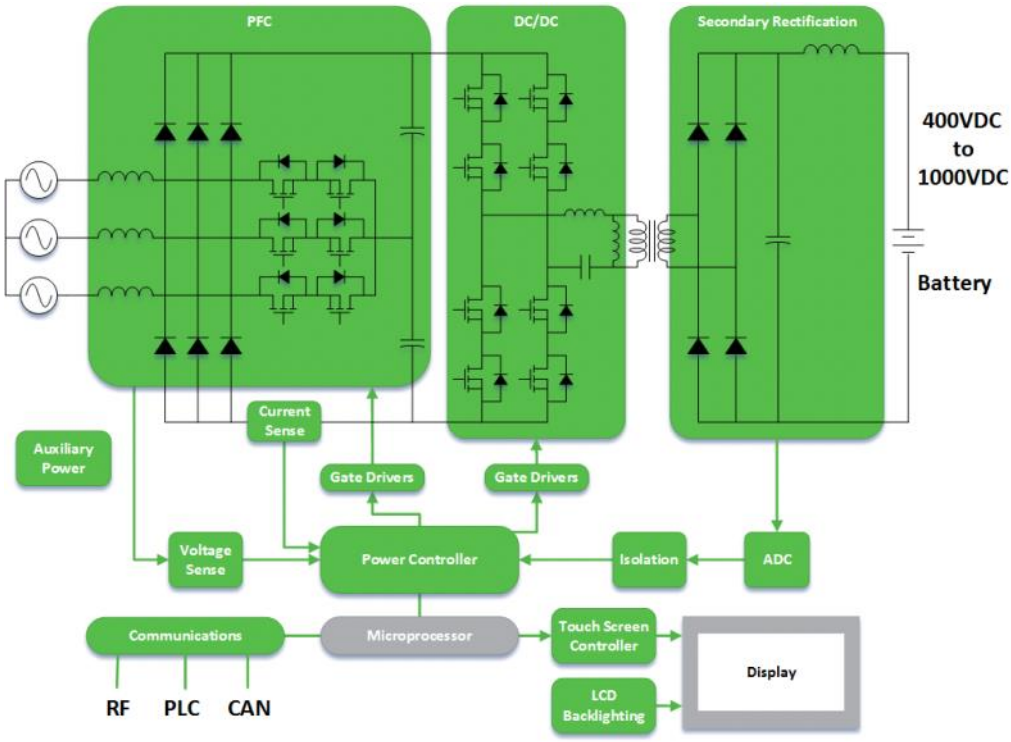
3.2 Three-phase PFC

For three-phase inputs, the ***Vienna rectifier*** is a popular PFC rectifier design [LY18, Sec. 4.6].

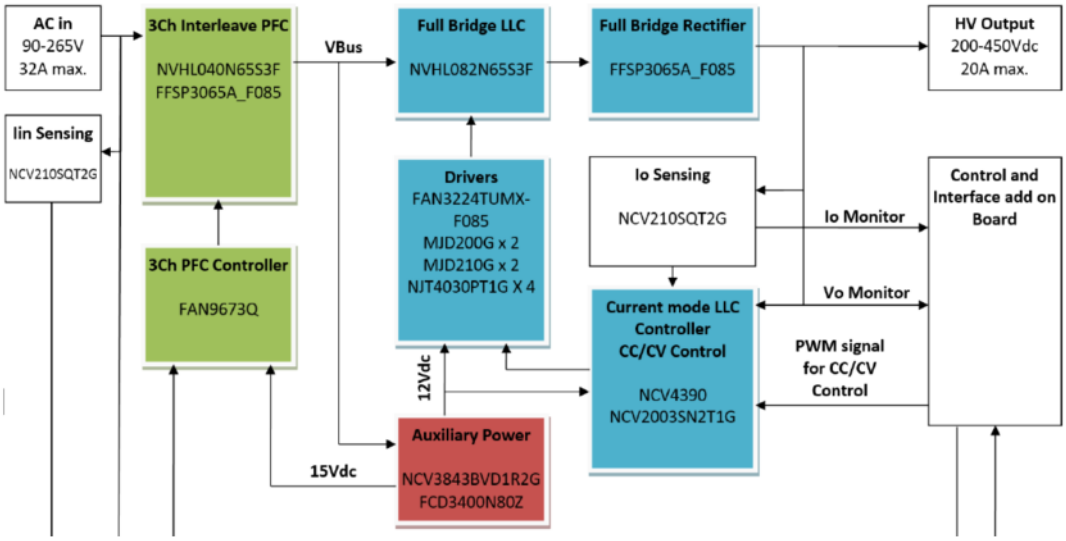
The converter draws high-quality sinusoidal supply currents and maintains good DC-link voltage regulation under wide load variation.



Widely used for EV battery charging. Example [ONS20] below shows a Vienna rectifier serving as the PFC stage of a charger:



The DC/DC converter above is a power-efficient *full-bridge LLC resonant* DC/DC converter (see also figure below), whose LLC resonant network serves as a filter of higher odd harmonics of the input square wave [WDK14].



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Saturday, 21 May 2022 3:06 PM

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